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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/957,395	09/19/2001	Anisul Khan	AM5782	4481

7590

02/24/2004

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EXAMINER

CULBERT, ROBERTS P

ART UNIT PAPER NUMBER

1763

DATE MAILED: 02/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/957,395	KHAN ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Roberts Culbert	1763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 12/24/03.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 5-20 is/are rejected.
- 7) ☒ Claim(s) 4 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 September 2001 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

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## **DETAILED ACTION**

### ***Response to Arguments***

Applicant's arguments with respect to the Sume reference have been considered but are moot in view of the new ground(s) of rejection.

Applicant has argued that Yallup does not teach or suggest processes related to forming an optical waveguide. The examiner respectfully disagrees with this assertion. Yallup is related to waveguide forming processes in that Yallup forms a structure suitable for a waveguide as would be recognized by one of ordinary skill in the art at the time of invention. Note for example, that U.S. Patent 5,604,835 to Nakamura teaches that polysilicon core and SiO<sub>2</sub> cladding materials are conventional in the waveguide fabrication art. See (Col. 9 Line 43 – Col. 10 line 14)

### ***Drawings***

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

There is no illustration in the drawings that shows a waveguide that is clad by the first insulating layer and the top cladding layer as recited in claim 15.

Claims 1 and 6 recite the method steps of forming an opening through said semiconductor layer to said first insulating layer and filling said opening with a core material. It is noted that the step of depositing a first cladding conformally in said opening has been omitted. It is further noted that the opening is not "filled" with a core material in any of the illustrated embodiments of the invention. Instead the drawings only illustrate filling the opening with both a conformal cladding layer and a core material.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

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***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 6-12, 14, 15 and 16-20 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6, recites the method step "planarizing the core to remove said silicon oxide layer"

It is not clear if the claim is indicating that the oxide layer is partially removed since complete removal is not illustrated in the drawings or described in the specification. See Fig. 5f.

Claims 9 and 20 are not clear because the method step is not positively recited. It is suggested, for example, that Claim 9 be reworded to recite the method step as in Claim 8.

Claim 14 recites the limitation "wherein the bottom cladding layer..." There is insufficient antecedent basis for the limitation in the claim.

***Double Patenting***

Applicant is advised that should claim 8 be found allowable, claim 20 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

***Claim Rejections - 35 USC § 102***

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

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only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**Claims 1- 3 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,877,065 to Yallup.**

Yallup teaches a method of making an isolation trench in a silicon substrate material comprising providing a substrate comprising a silicon semiconductor layer (10) disposed on a first insulating layer (34); forming an opening through said semiconductor layer to said first insulating layer (Figure 3); conformally depositing a bottom cladding layer in the opening (Col. 3, Lines 12-14), filling said opening with a core material (Col. 3, Lines 15-20); removing excess core material (Col. 3, Lines 20-22) and depositing a top cladding layer (18) over the core material (Col. 3, Lines 42-43).

Although Yallup does not teach that the trench isolation structure may be used as a waveguide, the recitation of this feature is only seen as intended use. The structure formed by Yallup is a waveguide based on the shape, form, and materials used.

Note that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

**Claims 1, 5, and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,282,358 to Hornbeck.**

Hornbeck teaches a method of making an optical waveguide comprising providing a substrate comprising a semiconductor layer (26a) disposed on a first insulating layer (26b); forming an opening through said semiconductor layer to said first insulating layer (Figure 4); conformally depositing a bottom cladding layer in the opening (Figure 5), filling said opening with a core material (Figure 6); removing excess core material (Figure 7) and depositing a top cladding layer over the core material.

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Regarding claim 5, the excess core material is removed by chemical-mechanical polishing.

Regarding Claim 9, Hornbeck teaches that the substrate may comprise a semiconductor layer disposed on a first insulating layer disposed on a second insulating layer. (Col. 7, Lines 18-25)

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

**Claims 6-8, and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,877,065 to Yallup and in further view of the publication to Wolf, "*Silicon Processing for the VLSI Era*" pages 182-185, 191-192 and 219-220 and in further view of U.S. Patent 6,282,358 to Hornbeck.**

Regarding Claims 6 and 7, Yallup teaches the method of the invention substantially as claimed, but does not teach the use of a silicon oxide layer over a silicon nitride layer as a hard mask. However, Yallup teaches that it is known in the prior art to form a trench in a (SOI) substrate using a hard-mask (30). The hard mask is patterned using a photoresist. (Col. 3, Lines 2-3) The hard-mask is removed prior to the deposition of the top oxide layer by etching. (Col. 3, Line 38)

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Wolf teaches that it is known in the semiconductor art to use a hard-mask of silicon nitride and silicon oxide for the selective oxidation of Si. It would have been obvious to one of ordinary skill in the art at the time of invention to form a hard-mask on the silicon surface by depositing a silicon nitride layer and a silicon oxide layer in order to provide mechanical protection, and diffusion protection (passivation) with less likelihood of delaminating or cracking. The silicon nitride protects the underlying Si from oxidizing, while allowing a thermal SiO<sub>2</sub> layer to grow on regions of exposed Si. (See page 192 lines 5-6).

Yallup in view of Wolf fails to teach that the step of removing the core material results in the removal of the silicon oxide layer. However, Hornbeck teaches that a both the core material and the bottom cladding layer of a channel waveguide may be removed using CMP (planarizing). See Figure 7, and (Col. 7, Lines 52-57). It would have been obvious to one of ordinary skill in the art at the time of invention to use CMP to remove the excess core material in order to form a substantially planar surface for the core as it is well known in the art that a smooth core material reduces light-signal transmission losses in the wave-guide. Provided the combined teachings of Wolf Yallup and Hornbeck, It would have been obvious to one of ordinary skill in the art at the time of invention to remove the oxide layer of the hard mask of Wolf using planarization while removing the excess core material as shown by Hornbeck since doing so would eliminate extra steps in producing a waveguide structure consisting of a core material surrounded by a u-shaped bottom cladding as shown by Hornbeck.

Regarding Claims 8 and 20, Yallup teaches the use of a SOI substrate in order to provide an etch-stop for the trench formation process (Col. 3, Lines 7-10). Hornbeck also teaches that this step is conventional in the art of forming waveguides. (Col. 7, Lines 18-25) It would have been obvious to one of ordinary skill in the art at the time of invention to form the waveguide on a substrate comprising a semiconductor layer deposited on a first insulating layer deposited on a second insulating layer as taught by Hornbeck in order to provide an etch-stop layer for trench formation as this step is entirely conventional in the art.

Regarding Claims 16 and 17, Yallup teaches that the core is polysilicon and the bottom cladding silicon oxide which inherently possesses a different refractive index.

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Regarding Claim 18, Wolf teaches that it is conventional in the art of forming a silicon oxide films to deposit a layer conformally in a trench and over the surface of the substrate using chemical vapor deposition (CVD). See Figure 17 on Page 185. It would have been obvious to one of ordinary skill in the art at the time of invention to deposit the silicon oxide film of Yallup using CVD conformally in the trench and over the surface of the substrate as shown by Wolf as an alternative method to thermally grown oxide. As one of ordinary skill in the art appreciates, CVD deposited oxide films provide flexibility in modifying index of refraction, dopants and deposition temperatures. See Wolf p.183 for example.

Using the equivalent method of CVD for the oxide layer formation in the invention of Yallup, as modified by the hard mask layers taught by Wolf, requires additionally that the oxide be removed from the top surfaces of the semiconductor substrate and hard mask layers. Given this necessity, It would have been obvious to one of ordinary skill in the art at the time of invention to remove this layer during the planarization process of the core in order to eliminate extra steps in producing a waveguide structure consisting of a core material surrounded by a u-shaped bottom cladding as shown by Hornbeck.

Regarding Claim 19, as applied above, Yallup in view of Wolf and Hornbeck teaches the method of the invention substantially as claimed, but do not explicitly teach a first insulating layer comprised of glass or silicon oxide. Yallup does teach that the first insulating layer (34) is an oxide layer. It may be assumed that the layer is a silicon oxide layer as is conventional in the art of forming devices on (SOI) substrates.

**Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,877,065 to Yallup and in further view of U.S. Patent 6,553,170 to Zhong.**

As applied above, Yallup teaches the method of the invention substantially as claimed but does not teach that the top and bottom cladding layers may have a different refractive index.

However it is understood in the waveguide fabrication art that the top and bottom cladding layers may have a different refractive index as long as both layers have a lower refractive index than the core layer. Zhong teaches a method of forming a wave-guide having top and bottom cladding layers each with a different refractive index. The top clad (411) is Boron doped, and the bottom clad (412) is SiO<sub>2</sub> (Col. 5,



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Lines 3-5). It would have been obvious to one of ordinary skill in the art at the time of invention to form the cladding layers each with a different refractive index in order to improve the re-flow characteristics of the top clad layer and thereby improve the gap-filling properties of the top clad as taught by Zhong (Col. 2, Lines 55-61).

**Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,877,065 to Yallup and in further view of U.S. Patent 3,934,061 to Keck et al.**

As applied above, Yallup teaches the method of the invention substantially as claimed but does not teach that the bottom cladding layer is formed of glass:

Yallup does teach that the bottom cladding layer is made from SiO<sub>2</sub>, which may be assumed to be glass. Nevertheless, Keck teaches that the use of glass for cladding layers is old and well known in the waveguide fabrication art. It would have been obvious to one of ordinary skill in the art at the time of invention to form the cladding layer using the conventional materials such as glasses.

#### ***Allowable Subject Matter***

Claims 4 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 10-12 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

#### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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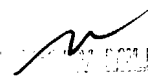
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberts Culbert whose telephone number is (571) 272-1433. The examiner can normally be reached on Monday-Friday (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory Mills can be reached on (571) 272-1439. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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